SM5842AP/APT

High-Class Audio Multi-function Digital Filter

OVERVIEW

The SM5842AP/APT is a multi-function digital filter IC, fabricated using NPC's Molybdenum-gate CMOS process, for digital audio reproduction equipment. It features 8-times oversampling (interpolation), independent left and right-channel digital deemphasis, and soft muting functions. It accepts 16, 18, 20 or 24-bit input data, and outputs data in 18, 20, 22 or 24-bit format. It operates using either a 384fs or 256fs system clock at sampling frequencies up to 48kHz + 10% (384fs SM5842AP, 384/256fs SM5842APT).

FEATURES

Functions

- L/R 2-channel processing
- 8-times oversampling (interpolation)
  - ≤ ±0.00002dB passband ripple
  - ≥ 117dB stopband attenuation
- Digital deemphasis
  - 32/44.1/48kHz sampling frequency (fs)
  - 2-channel independent ON/OFF control
- Soft muting
  - 2-channel independent ON/OFF control
- Input data format
  - 2s complement, MSB first
    - LR alternating, 16/18/20/24-bit serial, trailing data
    - LR alternating, 24-bit serial, leading data
    - LR simultaneous, 24-bit serial, leading data
- Output data format
  - 2s complement, MSB first, LR simultaneous
  - 18/20/22/24-bit serial
  - BCKO burst (NPC format)
- Dither round-up processing
  - ON (dither rounding)/OFF (normal rounding) control
- 25-bit internal data length
- Jitter-free function for correct operation in the presence of jitter between the system clock and LRCI clock
  - ON (jitter-free mode)/OFF (sync mode) control
- 256fs/384fs system clock selectable
  - 384fs
    - 21.2MHz maximum frequency (at maximum fs = 55.2kHz)
  - 256fs
    - 13MHz maximum frequency (at maximum fs = 50.7kHz, SM5842AP)
    - 14.2MHz maximum frequency (at maximum fs = 55.2kHz, SM5842APT)
- Crystal oscillator circuit built-in
- TTL-compatible input/outputs
- 5.0 ± 0.25V supply
- Molybdenum-gate CMOS process
- Package: 28-pin plastic DIP

Filter Configuration

- Linear phase 3-stage FIR interpolation filter
  - 169-tap 1st stage (fs to 2fs)
  - 29-tap 2nd stage (2fs to 4fs)
  - 17-tap 3rd stage (4fs to 8fs)
- Deemphasis filter
  - IIR filter configuration for accurate gain and phase characteristics
- 26 × 24-bit parallel multiplier/32-bit accumulator for high precision
- Overflow limiter built-in

APPLICATIONS

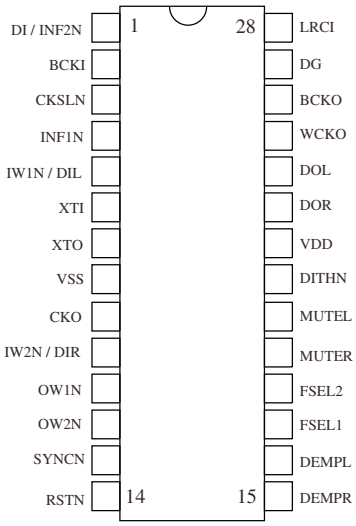
- CD players
- DAT players
- PCM systems

ORDERING INFORMATION

Device	Package
SM5842AP	28-pin DIP
SM5842APT	

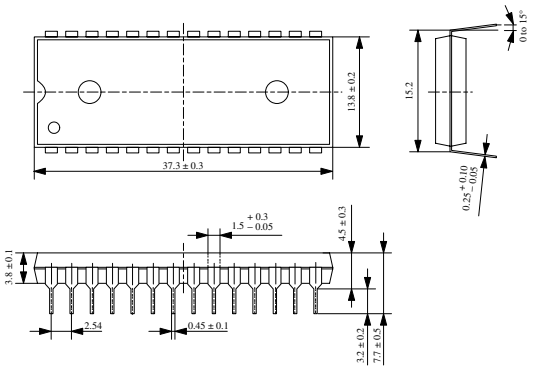
PINOUT

(Top view)

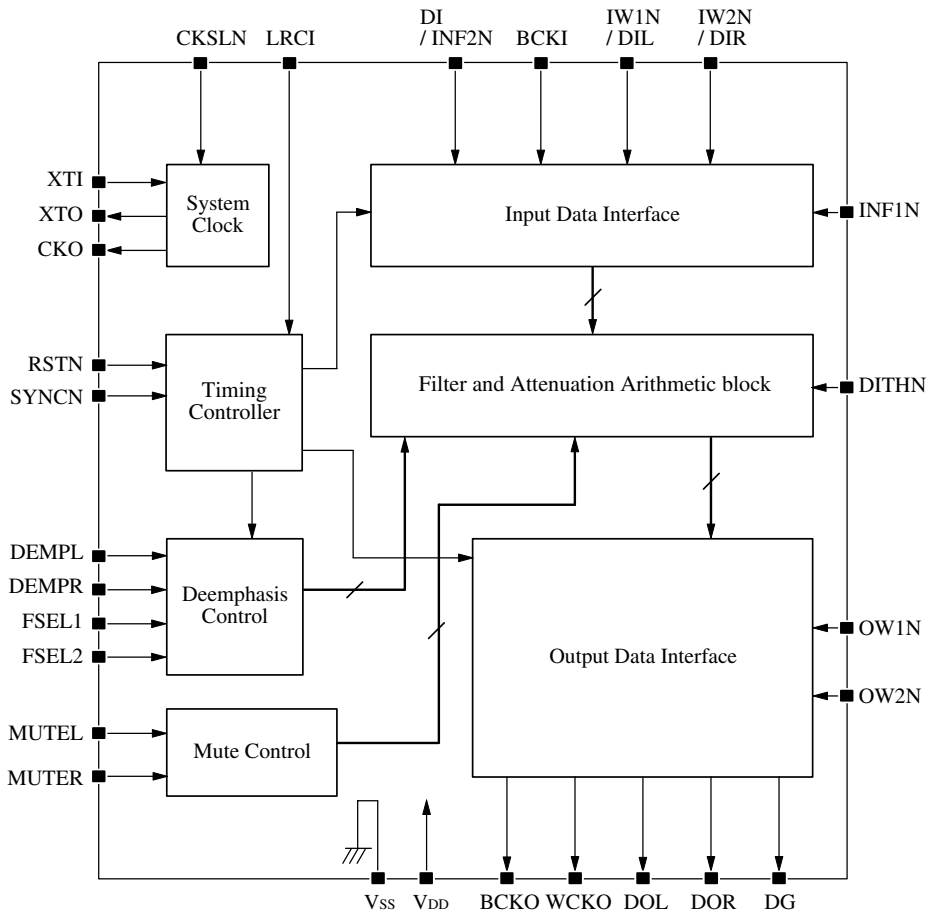


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>Number</th><th>Name</th><th>I/O[1]</th><th>Description</th></tr>
<tr><td>1</td><td>DI/INF2N</td><td>Ip</td><td>Data input when INF1N is LOW, and input format select pin 2 when INF1N is HIGH.</td></tr>
<tr><td>2</td><td>BCKI</td><td>Ip</td><td>Input bit clock</td></tr>
<tr><td>3</td><td>CKSLN</td><td>Ip</td><td>Oscillator and system clock select input. 384fs when HIGH, and 256fs when LOW.</td></tr>
<tr><td>4</td><td>INF1N</td><td>Ip</td><td>Input format select pin 1. INF1N and INF2N select the pin functions below.
<table>
<tr><th rowspan="2">INF1N</th><th rowspan="2">DI/INF2N</th><th rowspan="2">Input format</th><th colspan="3">Pin function selection</th></tr>
<tr><th>DI/INF2N</th><th>IW1N/DIL</th><th>IW2N/DIR</th></tr>
<tr><td>LOW</td><td>LOW</td><td rowspan="2">LR alternating, trailing data</td><td rowspan="2">DI</td><td rowspan="2">IW1N</td><td rowspan="2">IW2N</td></tr>
<tr><td>LOW</td><td>HIGH</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>LR alternating, leading data</td><td rowspan="2">INF2N</td><td rowspan="2">DIL</td><td rowspan="2">DIR</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>LR simultaneous, leading data</td></tr>
</table></td></tr>
<tr><td>5</td><td>IW1N/DIL</td><td>Ip</td><td>Input bit length select pin 1 when INF1N is LOW, and left-channel data input when INF1N is HIGH. IW1N and IW2N select the input data length.
<table>
<tr><th>INF1N</th><th>IW2N/DIL</th><th>IW1N/DIR</th><th>Input bit length</th></tr>
<tr><td rowspan="4">LOW</td><td>LOW</td><td>LOW</td><td>24 bits</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>20 bits</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>18 bits</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>16 bits</td></tr>
<tr><td>HIGH</td><td>×</td><td>×</td><td>24 bits</td></tr>
</table></td></tr>
<tr><td>6</td><td>XTI</td><td>I</td><td>Oscillator input connection</td></tr>
<tr><td>7</td><td>XTO</td><td>O</td><td>Oscillator output connection</td></tr>
<tr><td>8</td><td>VSS</td><td>–</td><td>Ground</td></tr>
<tr><td>9</td><td>CKO</td><td>O</td><td>Oscillator output clock. Same frequency as XTI.</td></tr>
<tr><td>10</td><td>IW2N/DIR</td><td>Ip</td><td>Input bit length select pin 2 when INF2N is LOW, and right-channel data input when INF2N is HIGH. IW1N and IW2N select the input data length as shown in the table for pin 5.</td></tr>
<tr><td>11</td><td>OW1N</td><td>Ip</td><td rowspan="2">Output length select bits.
<table>
<tr><th>OW2N</th><th>OW1N</th><th>Output bit length</th></tr>
<tr><td>LOW</td><td>LOW</td><td>24 bits</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>22 bits</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>20 bits</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>18 bits</td></tr>
</table></td></tr>
<tr><td>12</td><td>OW2N</td><td>Ip</td></tr>
<tr><td>13</td><td>SYNCN</td><td>Ip</td><td>Sync mode select pin. Normal sync mode when LOW, and jitter-free mode when HIGH.</td></tr>
<tr><td>14</td><td>RSTN</td><td>Ip</td><td>System reset. Reset operation when LOW, and normal operation when HIGH.</td></tr>
<tr><td>15</td><td>DEMPR</td><td>Ip</td><td>Right-channel deemphasis control signal. OFF when LOW, and ON when HIGH.</td></tr>
<tr><td>16</td><td>DEMPR</td><td>Ip</td><td>Left-channel deemphasis control signal. OFF when LOW, and ON when HIGH.</td></tr>
<tr><td>17</td><td>FSEL1</td><td>Ip</td><td rowspan="2">Deemphasis filter select inputs
<table>
<tr><th>FSEL1</th><th>FSEL2</th><th>Sampling frequency (fs)</th></tr>
<tr><td>LOW</td><td>LOW</td><td>44.1kHz</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>48kHz</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>Invalid setting</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>32kHz</td></tr>
</table></td></tr>
<tr><td>18</td><td>FSEL2</td><td>Ip</td></tr>
</table>

Number	Name	I/O[1]	Description
19	MUTER	Ip	Right-channel mute signal. Muting when HIGH, and normal output when LOW.
20	MUTEL	Ip	Left-channel mute signal. Muting when HIGH, and normal output when LOW.
21	DITHN	Ip	Dither processing control. ON when LOW, and OFF when HIGH.
22	VDD	–	5V supply
23	DOR	O	Right-channel data output
24	DOL	O	Left-channel data output
25	WCKO	O	Output word clock
26	BCKO	O	Output bit clock
27	DG	O	Deglitched output
28	LRCI	Ip	Input data sample rate (fs) clock

1. I = input, Ip = Input with pull-up resistor, O = output

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–40 to 125	°C
Power dissipation	P_D	550	mW

Recommended Operating Conditions

V_{SS} = 0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		4.75 to 5.25	V
Operating temperature range	T_{opr}	SM5842AP	–20 to 80	°C
		SM5842APT	–20 to 70	

DC Electrical Characteristics

V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = –20 to 80°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}	V_{DD} = 5.0V[1]	–	60	80	mA
XTI HIGH-level input voltage	V_{IH1}		0.7V_{DD}	–	–	V
XTI LOW-level input voltage	V_{IL1}		–	–	0.3V_{DD}	V
HIGH-level input voltage[2]	V_{IH2}		2.4	–	–	V
LOW-level input voltage[2]	V_{IL2}		–	–	0.5	V
HIGH-level output voltage[3]	V_{OH1}	I_{OH} = –0.4mA	2.5	–	–	V
LOW-level output voltage[3]	V_{OL1}	I_{OL} = 1.6mA	–	–	0.4	V
XTO HIGH-level output voltage	V_{OH2}	I_{OH} = –1.0mA	V_{DD} – 0.5	–	–	V
XTO LOW-level output voltage	V_{OL2}	I_{OL} = 1.0mA	–	–	0.4	V
XTI HIGH-level input current	I_{LH}	V_{IN} = V_{DD}	–	10	20	µA
XTI LOW-level input current	I_{LL1}	V_{IN} = 0V	–	10	20	µA
LOW-level input current[2]	I_{LL2}	V_{IN} = 0V	–	10	20	µA
Input leakage current[2]	I_{IH}	V_{IN} = V_{DD}	–	–	1.0	µA

1. f_{SYS} = 256fs = 14.2MHz (CKSLN = LOW), no output load
2. Pins DI/INF2N, BCKI, CKSLN, INF1N, IW1N/DIL, IW2N/DIR, OW1N, OW2N, SYNCN, RSTN, DEMPR, DEMPL, FSEL1, FSEL2, MUTER, MUTEL, DITHN, LRCI
3. Pins CKO, DOL, DOR, BCKO, WCKO, DG

AC Electrical Characteristics

Input Clock (XTI: SM5842AP)

Crystal oscillator

fs = 384fs (CKSLN = HIGH): V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = −20 to 80°C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{OSC}	2.0	–	21.2	MHz

fs = 256fs (CKSLN = LOW): V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = −20 to 80°C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{OSC}	1.0	–	13.0	MHz

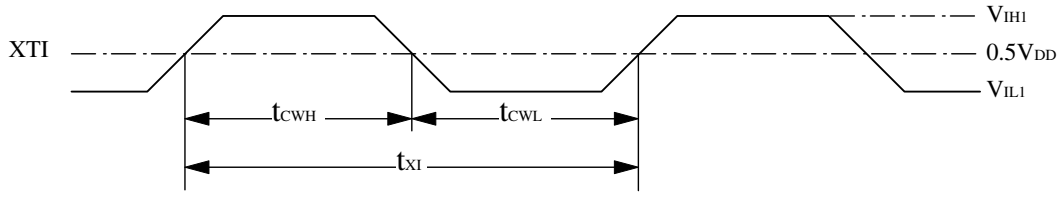
External clock input

fs = 384fs (CKSLN = HIGH): V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = −20 to 80°C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock HIGH-level pulsewidth	t_{CWH}	20	–	250	ns
Clock LOW-level pulsewidth	t_{CWL}	20	–	250	ns
Clock pulse cycle time	t_{XI}	47	–	500	ns

fs = 256fs (CKSLN = LOW): V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = −20 to 80°C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock HIGH-level pulsewidth	t_{CWH}	35	–	500	ns
Clock LOW-level pulsewidth	t_{CWL}	35	–	500	ns
Clock pulse cycle time	t_{XI}	76	–	1000	ns



Input Clock (XTI: SM5842APT)

Crystal oscillator

fs = 384fs (CKSLN = HIGH): V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = –20 to 70°C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{OSC}	2.0	–	21.2	MHz

fs = 256fs (CKSLN = LOW): V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = –20 to 70°C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{OSC}	1.0	–	14.2	MHz

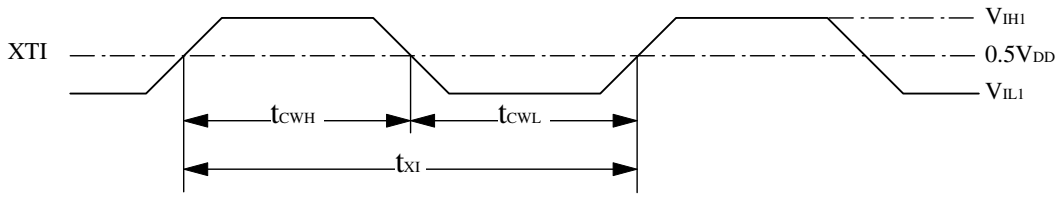
External clock input

fs = 384fs (CKSLN = HIGH): V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = –20 to 70°C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock HIGH-level pulsewidth	t_{CWH}	20	–	250	ns
Clock LOW-level pulsewidth	t_{CWL}	20	–	250	ns
Clock pulse cycle time	t_{XI}	47	–	500	ns

fs = 256fs (CKSLN = LOW): V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = –20 to 70°C

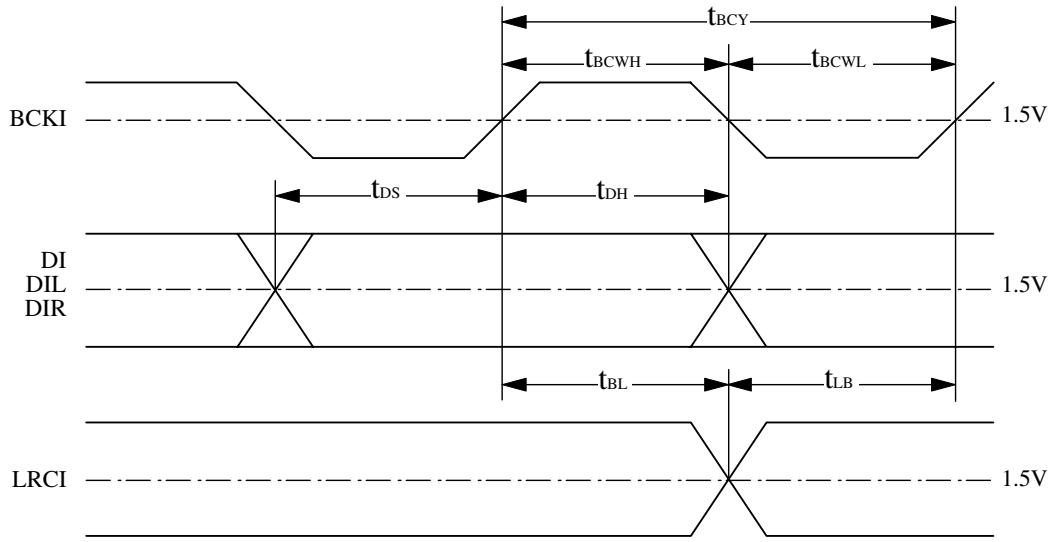
Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock HIGH-level pulsewidth	t_{CWH}	30	–	500	ns
Clock LOW-level pulsewidth	t_{CWL}	30	–	500	ns
Clock pulse cycle time	t_{XI}	70	–	1000	ns



Serial input timing (BCKI, DI, DIL, DIR, LRCI)

SM5842AP: V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = −20 to 80°C
SM5842APT: V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = −20 to 70°C

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns
BCKI pulse cycle	t_{BCY}	100	–	–	ns
DIN setup time	t_{DS}	50	–	–	ns
DIN hold time	t_{DH}	50	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BL}	50	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB}	50	–	–	ns



Reset timing (RSTN)

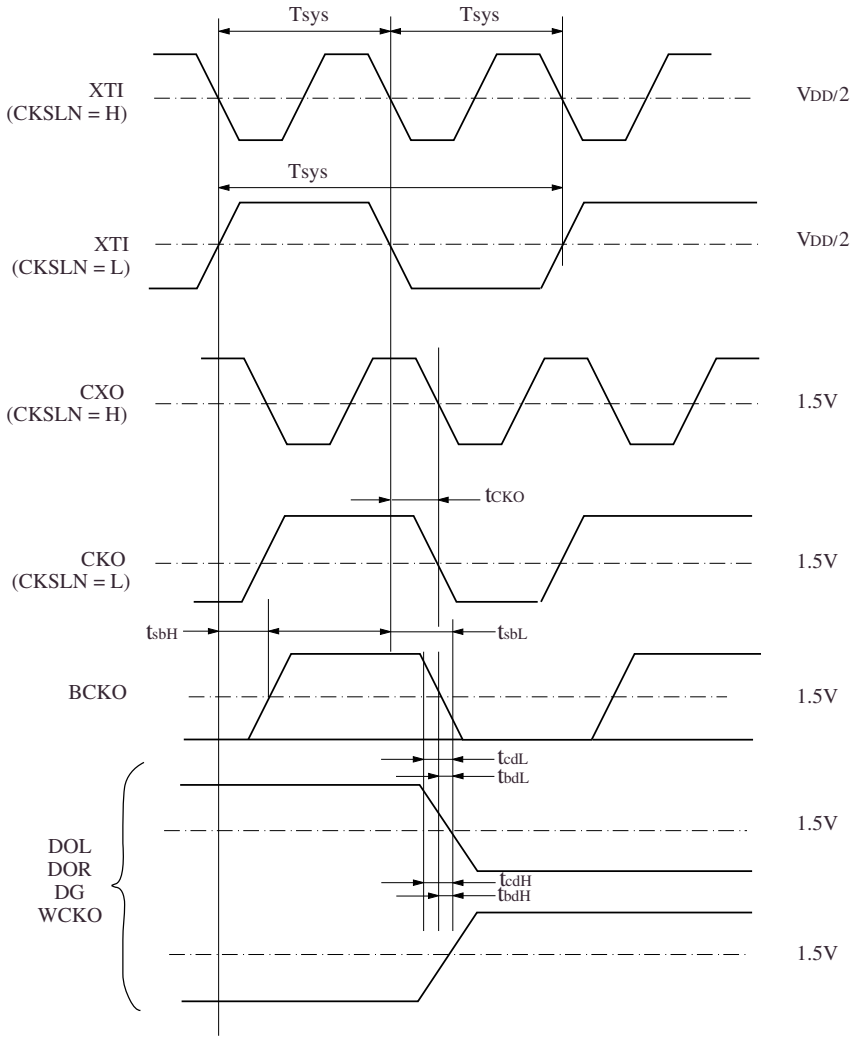
SM5842AP: V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = −20 to 80°C
SM5842APT: V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = −20 to 70°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
$\overline{RST}$ LOW-level reset pulsewidth	t_{RST}	At power-ON	1	–	–	µs
		At all other times	50	–	–	ns

Output timing

SM5842AP: V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = −20 to 80°C, C_L = 15pF
SM5842APT: V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = −20 to 70°C, C_L = 15pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
XTI to XTO delay	t_{XTO}	XTI fall to XTO rise	3	–	15	ns
XTI to CKO delay	t_{CKO}	XTI fall to CKO fall	10	–	35	ns
XTI to BCKO delay (CKSLN = HIGH)	t_{sbH}	XTI fall to BCKO rise	20	–	65	ns
	t_{sbL}	XTI fall to BCKO fall	20	–	65	
XTI to BCKO delay (CKSLN = LOW)	t_{sbH}	XTI fall to BCKO rise	20	–	65	ns
	t_{sbL}	XTI fall to BCKO fall	20	–	65	
BCKO to DOL, DOR, WCKO delay	t_{bdH}	BCKO fall to output rise	–5	–	10	ns
	t_{bdL}	BCKO fall to output fall	–5	–	10	
CKO to DOL, DOR, WCKO, DG delay	t_{cdH}	CKO fall to output rise	12	–	45	ns
	t_{cdL}	CKO fall to output fall	12	–	45	
XTO to DOL, DOR, WCKO, DG delay	t_{xdH}	XTO rise to output rise	15	–	50	ns
	t_{xdL}	XTO rise to output fall	15	–	50	

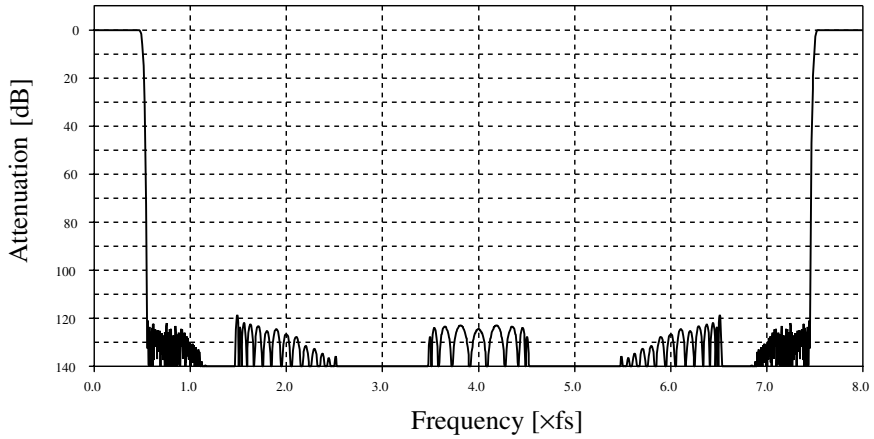


Filter Characteristics

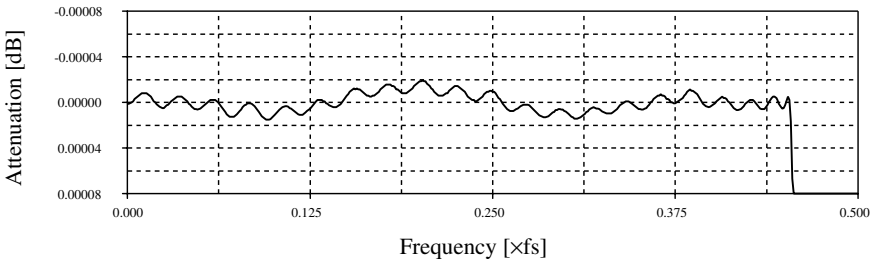
8-times interpolation filter

Parameter	Rating
Passband	0 to 0.4535fs
Stopband	0.5465fs to 7.4535fs
Passband ripple	≤ ±0.00002dB
Stopband attenuation	≥ 117dB
Group delay	Fixed

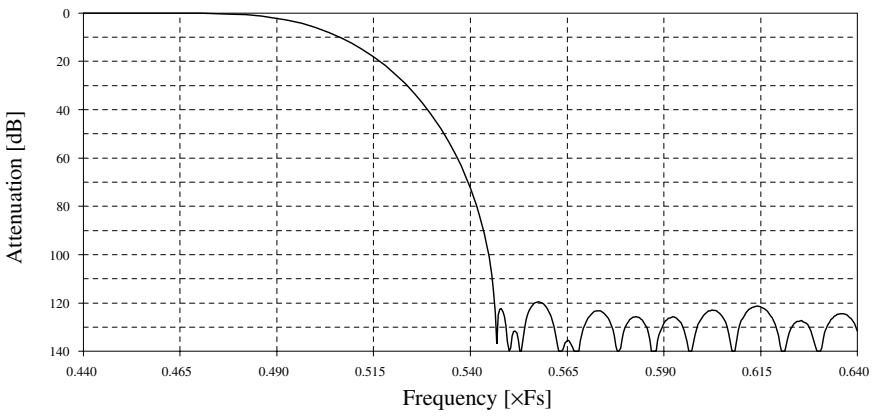
8fs filter response with deemphasis OFF



8fs filter passband response with deemphasis OFF



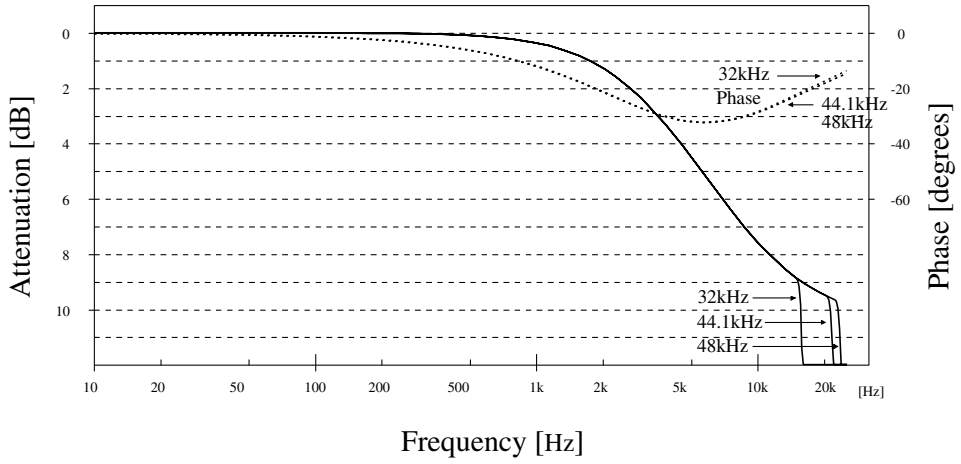
8fs filter transition response with deemphasis OFF



Deemphasis filter

Parameter		Sampling frequency (fs)		
		32kHz	44.1kHz	48kHz
Passband bandwidth [kHz]		0 to 14.5	0 to 20.0	0 to 21.7
Deviation from ideal characteristic	Attenuation	≤ ±0.001dB		
	Phase, θ	0 to 1.5°		

Passband response with deemphasis ON (logarithmic frequency axis)



FUNCTIONAL DESCRIPTION

The basic arithmetic block is shown in figure 1, and the function of each block is described in the following sections.

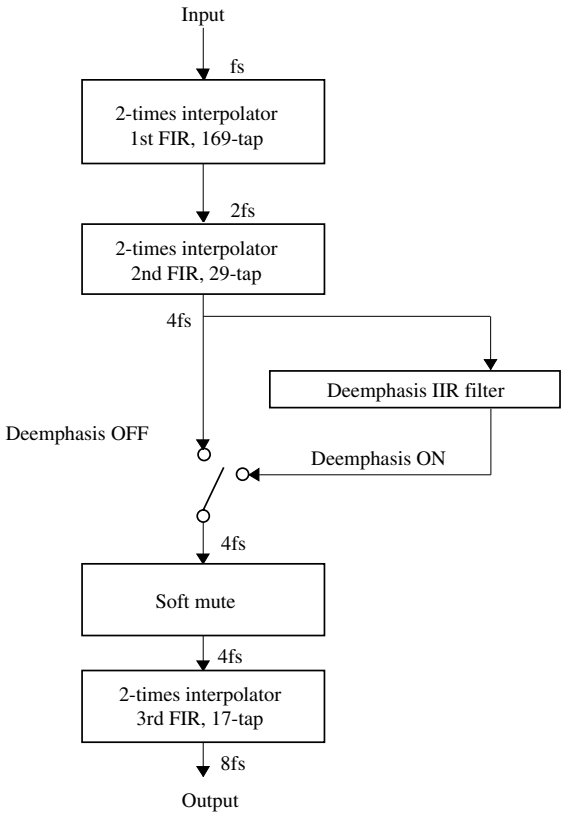


Figure 1. Arithmetic block diagram

8-times Oversampling (Interpolation)

The interpolation arithmetic block is comprised of 3 cascaded, 2-times FIR interpolation filters, as shown in figure 1.

The input signal is sampled at rate fs, and then 8-times oversampling data is output. Sampling noise in the 0.5465fs to 7.4535fs stopband is removed by the interpolation filter.

Digital Deemphasis

The digital deemphasis filter has the same construction as analog filters. It is implemented as an IIR filter to faithfully reproduce the gain and phase characteristics of standard analog deemphasis filters. The three sets of filter coefficients for the three fs = 32.0/44.1/48.0kHz sampling frequencies are selected by FSEL1 and FSEL2 when the sampling frequency is specified, as shown in table 1. Independent deemphasis for the left and right channel is controlled independently by DEMPL and DEMPR, respectively. Digital deemphasis is ON when DEMPL/DEMPR is HIGH, and OFF when DEMPL/DEMPR is LOW.

Table 1. Sampling frequency select

FSEL1	FSEL2	Sampling frequency (fs)
LOW	LOW	44.1kHz
LOW	HIGH	48kHz
HIGH	LOW	Invalid setting
HIGH	HIGH	32kHz

Soft Muting

Muting of the left and right channel is controlled independently by MUTEL and MUTER, respectively. Muting is ON when MUTEL/MUTER is HIGH, muting is OFF when MUTEL/MUTER is LOW.

When MUTEL/MUTER goes HIGH, the attenuation changes smoothly from 0 to −∞ dB in 512/fs, or approximately 11.6ms when fs = 44.1kHz. When MUTEL/MUTER goes LOW, muting is released and the attenuation changes smoothly from −∞ to 0dB, again taking approximately 11.6ms.

When RSTN goes LOW, the DOL and DOR outputs go LOW, immediately muting the output signal. Muting is released and timing is synchronized when RSTN goes HIGH.

System Clock (XTI, XTO, CKO, CKSLN)

Two system clock frequencies, 384fs and 256fs, can be used. An external clock source can be input on XTI, or a crystal oscillator can be constructed by connecting a crystal between XTI and XTO. The system clock is also buffered and then output on CKO. The system clock frequency selection and the internal clock frequency are shown in table 2.

Table 2. System clock frequency select

Parameter	CKSLN	
	HIGH	LOW
XTI input clock frequency ($f_{XI} = 1/t_{XI}$)	384fs	256fs
CKO clock frequency	384fs	256fs
Internal clock frequency (t_{SYS})	$2 \times t_{XI}$	t_{XI}

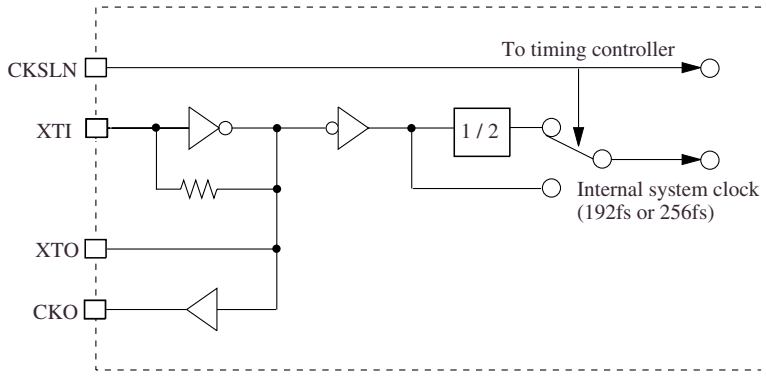


Figure 2. Clock generator circuit

Audio Data Input (INF1N, INF2N, IW1N, IW2N, DI, DIL, DIR, BCKI, LRCI)

The input data format and several input pin functions are selected by the state of INF1N and INF2N as shown in table 3.

Table 3. Pin function select

INF1N	DI/INF2N	Input format	Pin function selection		
			DI/INF2N	IW1N/DIL	IW2N/DIR
LOW	LOW	LR alternating[1], trailing data	DI	IW1N	IW2N
LOW	HIGH				
HIGH	LOW	LR alternating, leading data	INF2N	DIL	DIR
HIGH	HIGH	LR simultaneous[2], leading data			

1. Alternating left-channel and right-channel data input on a single input DI.
2. Simultaneous left-channel and right-channel data input on two inputs, DIL and DIR, respectively.

The input data word length is selected by the state of IW1N and IW2N when INF1N is LOW. 24-bit is selected when INF1N is HIGH.

Table 4. Input word length

INF1N	IW2N/DIL	IW1N/DIR	Input word length
LOW	LOW	LOW	24 bits
	LOW	HIGH	22 bits
	HIGH	LOW	18 bits
	HIGH	HIGH	16 bits
HIGH	×	×	24 bits

Jitter-free Function (SYNCN)

The arithmetic circuit and output control timing is derived from the system clock, and is therefore independent of the input LRCI and BCKI clocks. Accordingly, any jitter in the data input clock (LRCI and BCKI) does not cause jitter in the output.

Generally, the internal timing is synchronized to the LRCI input timing after a system reset release, when RSTN goes from LOW to HIGH, on the first LRCI clock start edge. If the input timing and LRCI start edge timing subsequently drift, the input timing is automatically resynchronized when the timing error exceeds a certain value. There are 2 timing error values at which resynchronization occurs, selected by the state of SYNCN.

Jitter-free mode (SYNCN = HIGH)

When SYNCN is HIGH, the timing error value is ±3/8 × (LRCI clock period). When the difference between the input timing and LRCI start edge position do not exceed this value, internal timing is not resynchronized and all functions continue to operate normally.

Sync mode (SYNCN = LOW)

When SYNCN is LOW, the timing error value is ±1 × (system clock period), which is a much smaller timing error tolerance than in jitter-free mode. In this mode, the internal timing is guaranteed to follow the LRCI clock timing within this tolerance, making this mode useful for systems constructed from a multiple number of SM5842AP/APT devices.

Note that resynchronization affects the internal operation and can generate a momentary click noise output.

Audio Data Output (DOL, DOR, BCKO, WCKO, OW20N)

The output data is in serial, simultaneous left and right-channel, 2s complement, MSB first, BCKO burst (NPC format) format. The output data word length is selected by the state of OW1N and OW2N as shown in table 5.

Table 5. Output word length select

OW1N	OW2N	Output word length
LOW	LOW	24 bits
LOW	HIGH	22 bits
HIGH	LOW	20 bits
HIGH	HIGH	18 bits

8fs serial data is output in sync with the falling edge of the internal system clock and BCKO clock. The output timing is determined by CKSLN and the output word length. When CKSLN is LOW, the output timing is the same for different output word lengths. Only the number of BCKO bit clock pulses word changes depending on the output word length selected. When CKSLN is HIGH, however, the output timing for 24-bit output mode starts 1 bit earlier than for 18/20/22-bit output mode.

Table 6. Output timing

Parameter	Symbol	CKSLN = HIGH	CKSLN = LOW
Bit clock rate	t_B	1/192fs	1/256fs
Data word length	t_{DW}	$24t_{SYS}$	$32t_{SYS}$

System Reset (RSTN)

Under normal operating conditions, the SM5842AP/APT does not need to be reset. However, it can be reset when you want to synchronize the LRCI clock and internal operation timing in jitter-free mode.

The system is reset by applying a LOW-level pulse on RSTN.

The arithmetic and output timing counters are reset on the first LRCI start edge after reset is released, as long as the XTI clock has already stabilized. The LRCI start edge is determined by the state of INF1N and INF2N. When INF1N is LOW or when both INF1N and INF2N are HIGH, the start edge is the rising edge. When INF1N is HIGH and INF2N is LOW, the start edge is the falling edge.

When RSTN is LOW, the DOL and DOR outputs are LOW, muting the output signal to an attenuation level of −∞.

The power-ON reset pulse can be applied by a microcontroller or, for systems where XTI and LRCI are stable at power-ON, by connecting a capacitor of about 300pF between RSTN and VSS. For systems that do not use a microcontroller, the capacitor must be chosen such that the XTI and LRCI clocks fully stabilize before RSTN goes from LOW to HIGH.

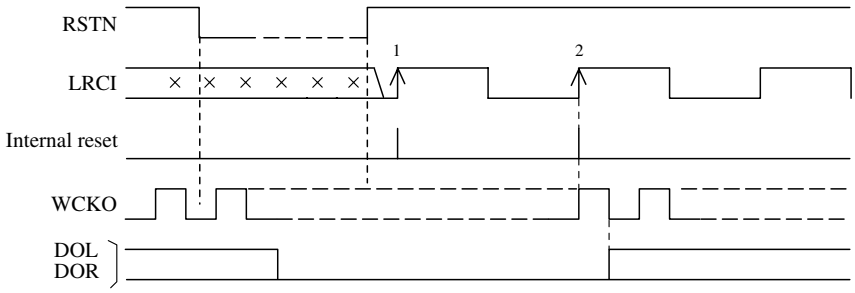
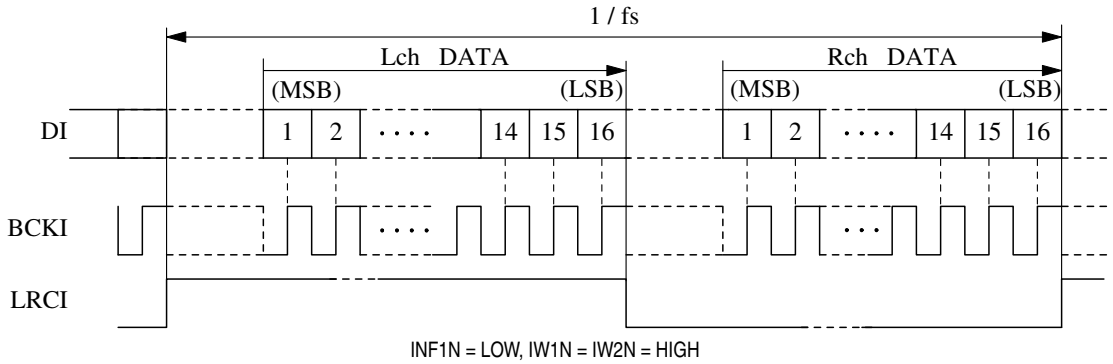


Figure 3. System reset timing and output muting

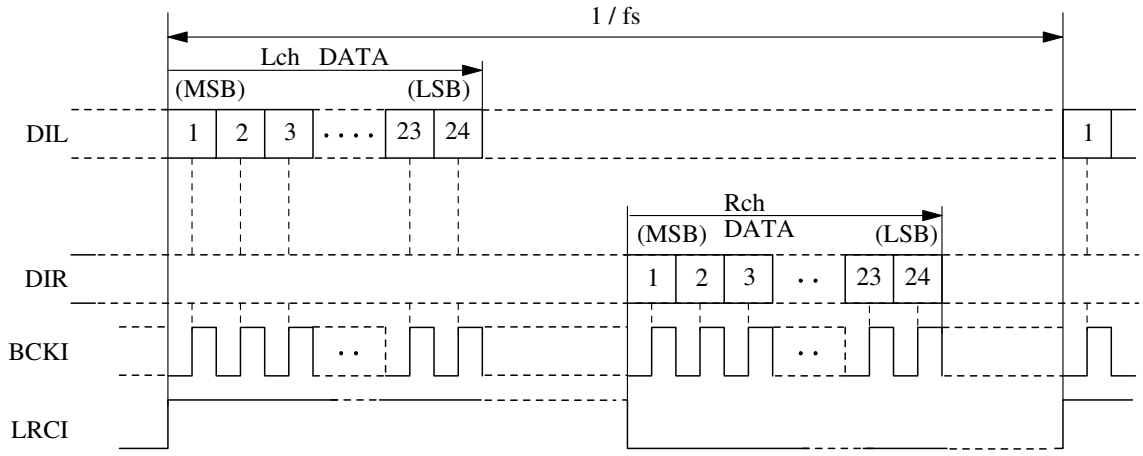
TIMING DIAGRAMS

Input Timing Examples (DIN, BCKI, LRCI)



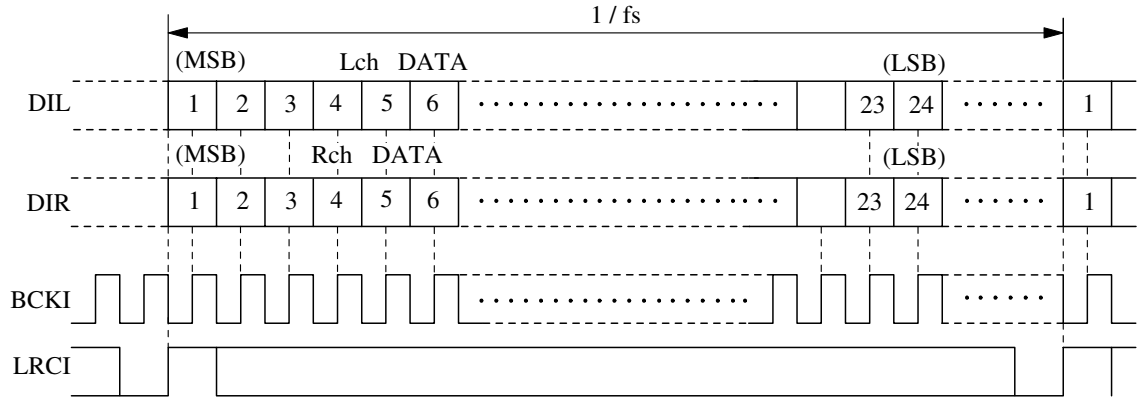
INF1N = LOW, IW1N = IW2N = HIGH

Figure 4. LR alternating, trailing data, 16-bit input



INF1N HIGH, INF2N = LOW.
Data following LSB is ignored. Requires minimum 24 BCKI clock pulses.

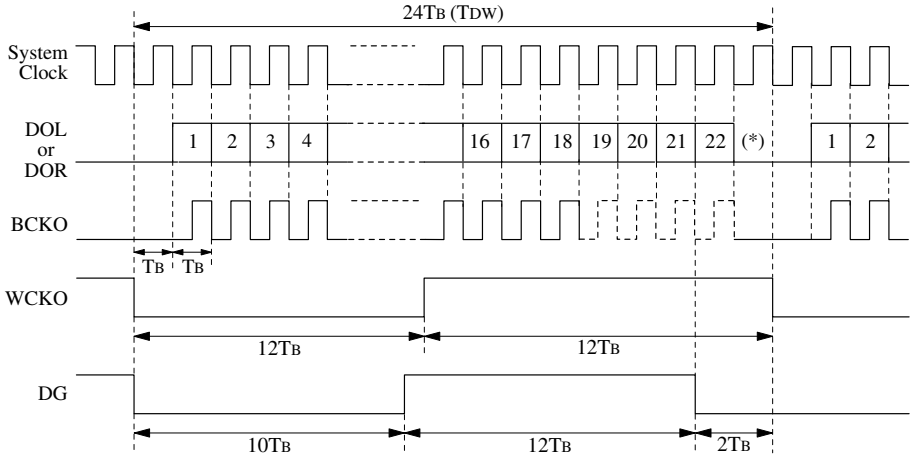
Figure 5. LR alternating, leading data, 24-bit input



INF1N = INF2N = HIGH.
Data following LSB is ignored. Requires minimum 24 BCKI clock pulses.

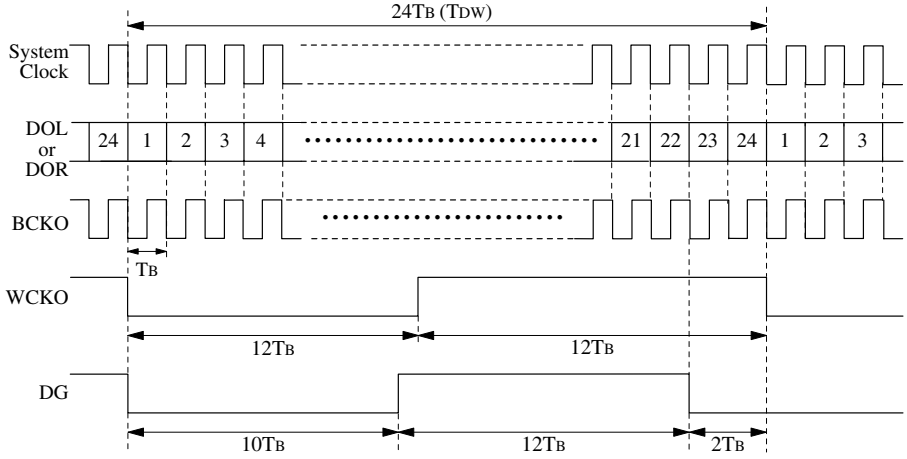
Figure 6. LR simultaneous, leading data, 20-bit input

Output Timing Examples (DOL, DOR, BCKO, WCKO, DG)



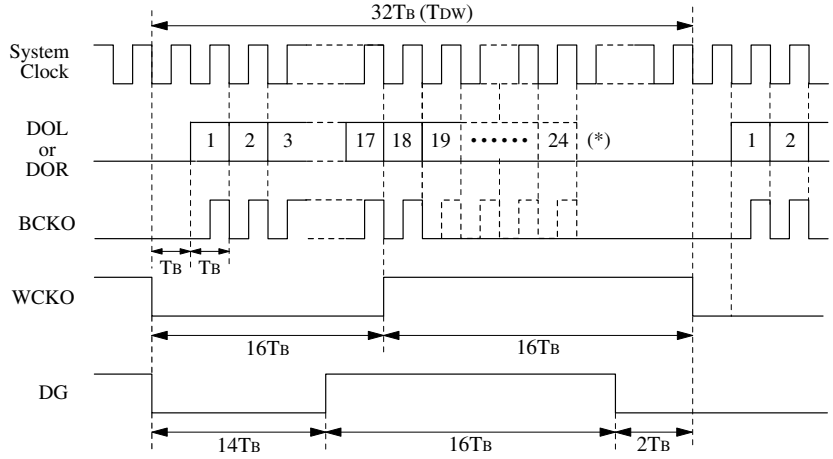
The number of output bits is determined by the output bit length selected.

Figure 7. 18/20/22-bit output (CKSLN = HIGH)



The number of output bits is determined by the output bit length selected.

Figure 8. 24-bit output (CKSLN = HIGH)



The number of output bits is determined by the output bit length selected.

Figure 9. 24-bit output (CKSLN = LOW)

Data Input to Output Delay Timing

This is the digital filter arithmetic computation time from the completion of data input at rate fs (t_{INPUT}) on the rising edge of LRCI to the start of data output at rate 8fs (t_{OUTPUT}) on the falling edge of WCKO.

Table 7. Output delay

CKSLN	SYNCN	Mode	$t_{OUTPUT} - t_{INPUT}$
LOW (256fs)	LOW	After reset + sync mode	48.625/fs
	HIGH	Jitter-free mode	48.25/fs – 49.0/fs
HIGH (384fs)	LOW	After reset + sync mode	48.75/fs
	HIGH	Jitter-free mode	48.375/fs – 49.125/fs

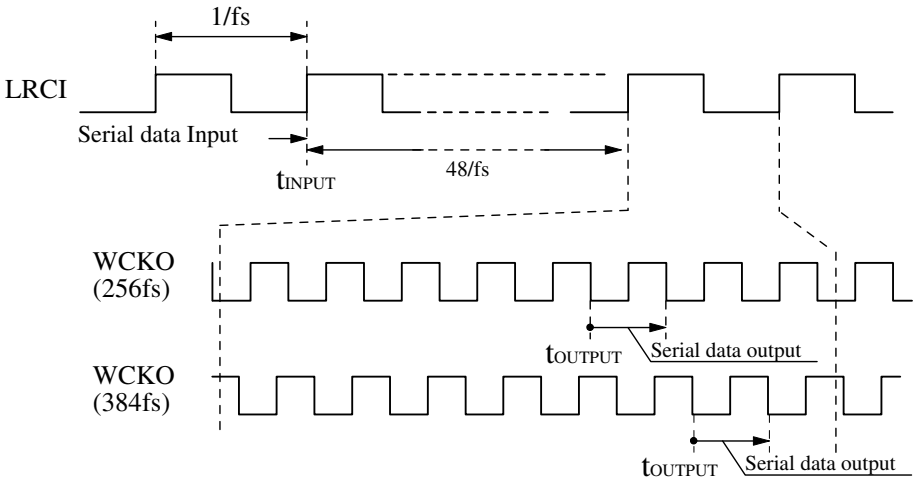


Figure 10. Delay timing 1

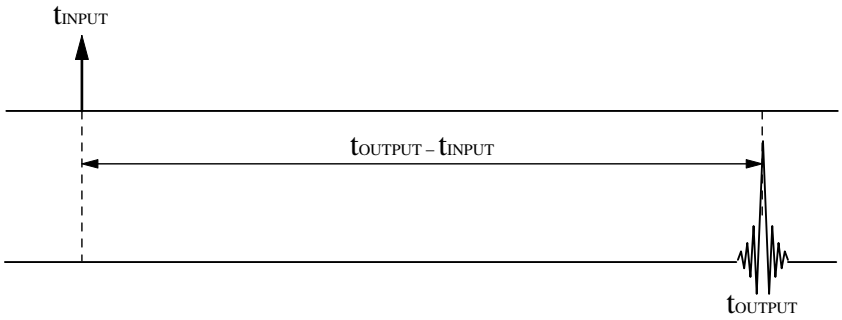
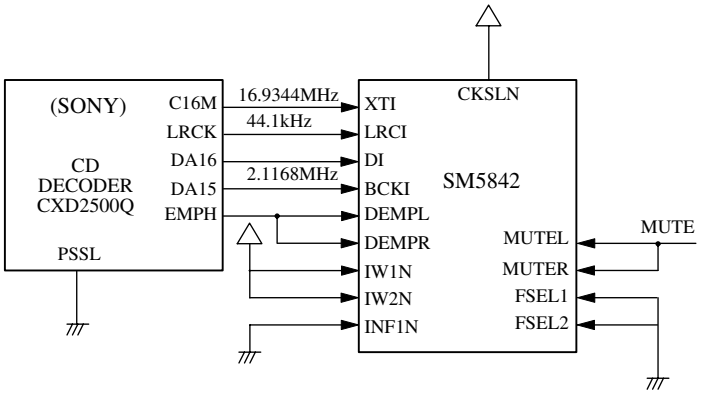


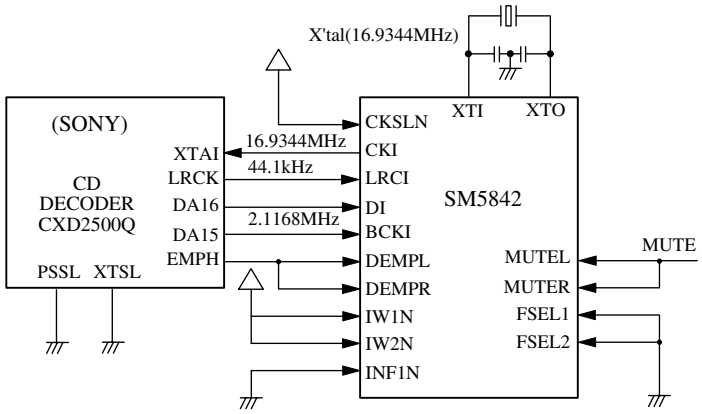
Figure 11. Delay timing 2

APPLICATION CIRCUITS

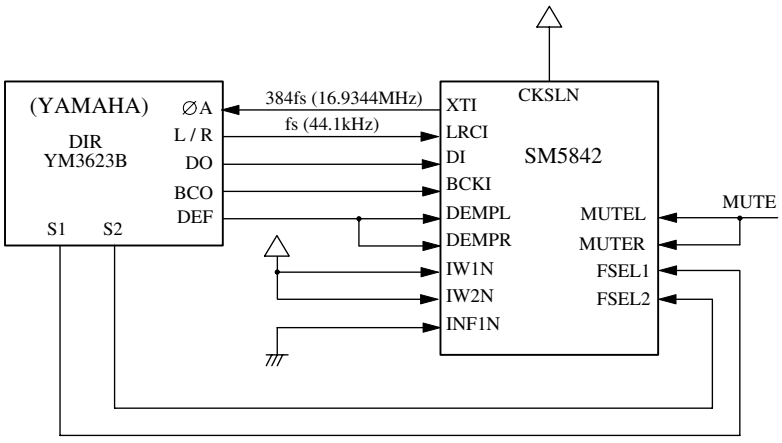
Input Interface Circuits

CD decoder (CXD2500Q) connection





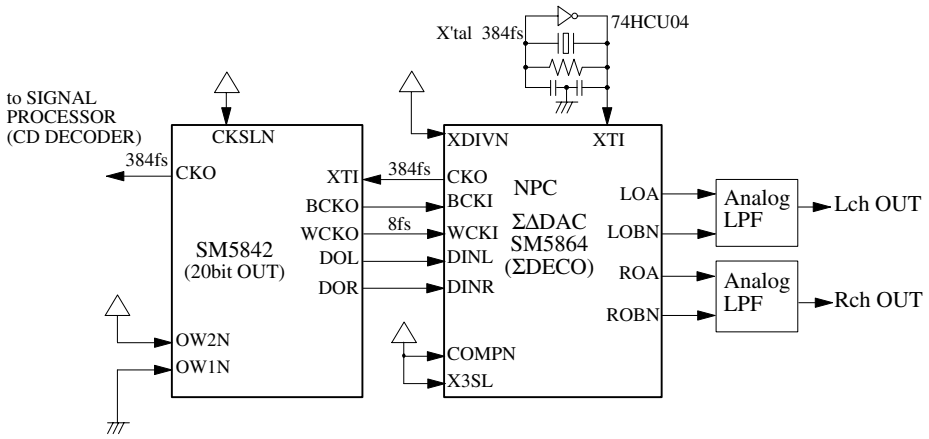
Digital audio interface receiver (YM3623B) connection



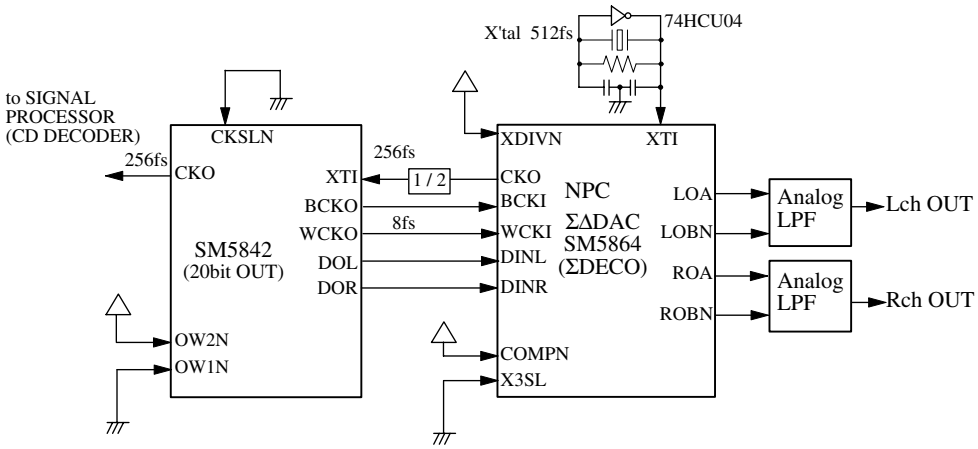
Output Interface Circuits

20-bit input ΣΔ DAC (SM5864AP) connection 1

384fs

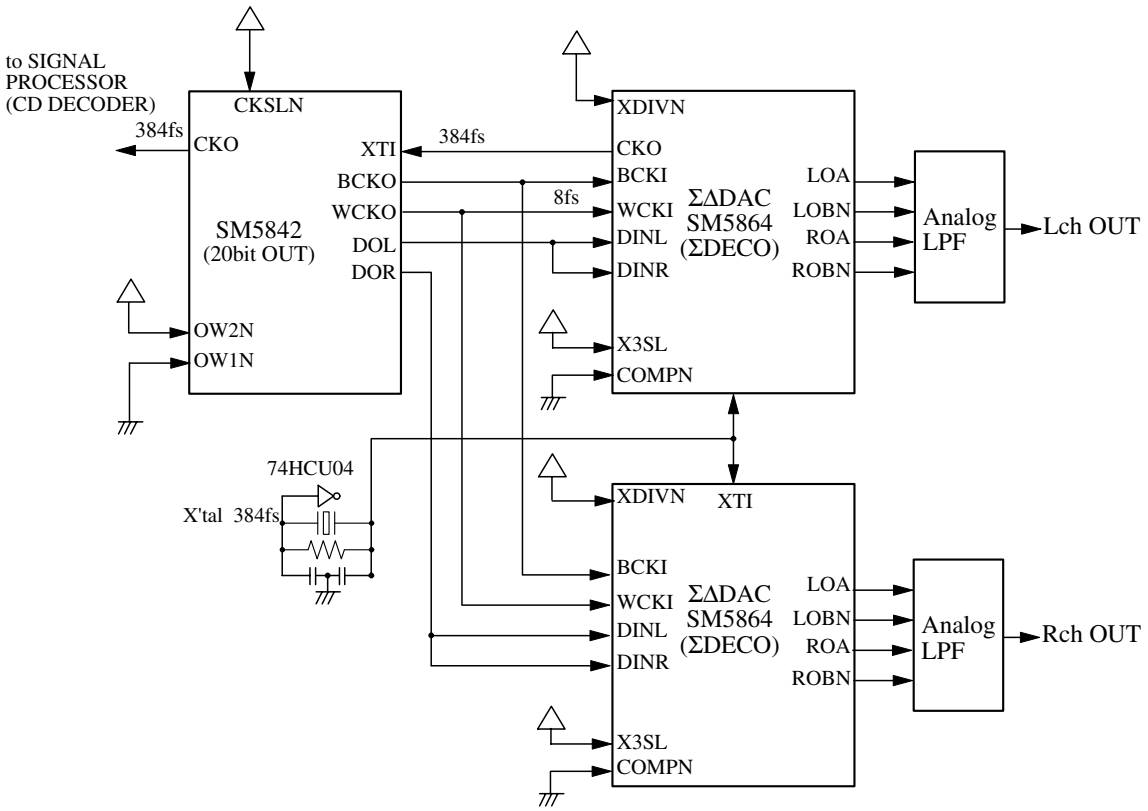


512fs



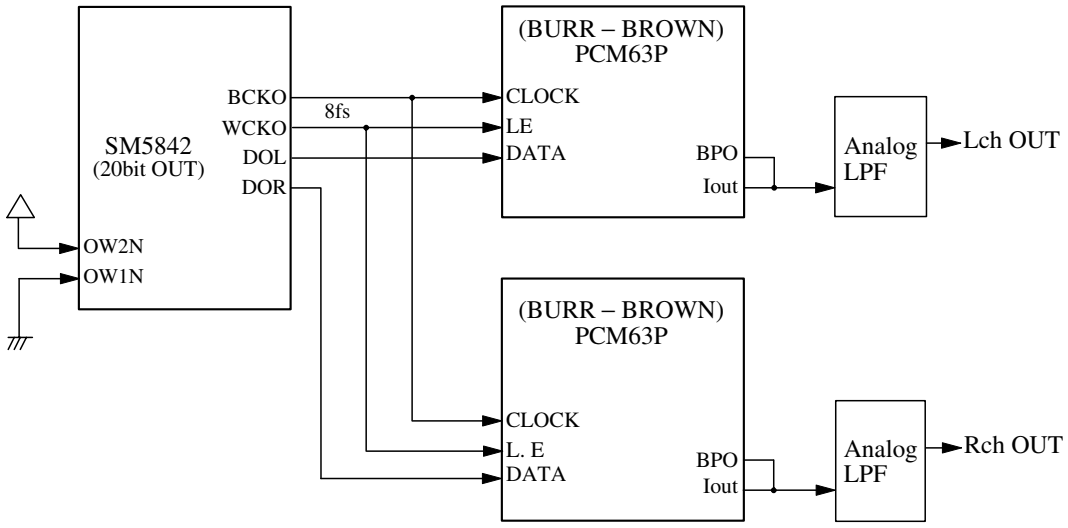
20-bit input ΣΔ DAC (SM5864AP) connection 2

L/R-channel independent complementary PWM output



20-bit input R–2R DAC (PCM63P) connection

L/R-channel independent



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